AMENDMENTS TO THE CLAIMS

Listing of claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1-13 (Cancelled)

14. (Original) A method of manufacturing a semiconductor device having a memory cell region and a peripheral region, comprising the steps of:

forming an alignment mark for positioning made of a conductive material, in said peripheral region;

forming a first insulating film so as to cover said alignment mark and extend to said memory cell region;

forming a second insulating film on said first insulating film;

forming a third insulating film on said second insulating film, said third insulating film having a low etching rate in relation to a first etchant for said first insulating film;

forming an opening portion so as to extend through said third and second insulating films up to said first insulating film;

forming a spacer on the side wall of said opening portion, said spacer having a low etching rate in relation to said first etchant for said first insulating film;

forming a first contact hole so as to extend through said first insulating film, using said third insulating film and said spacer as masks;

filling said opening portion and said first contact hole with a first conductive material to form a contact plug; and

selectively removing said third insulating film using a second etchant whose etching rate to said second insulating film is low.

15. (Original) A method according to claim 14, wherein said first, second, and third insulating films are transparent in relation to visible light.

16. (Original) A method according to claim 15, wherein said first insulating film is a silicon oxide film, said second insulating film is a silicon nitride film which grew through a low-pressure chemical vapor deposition process, and said third insulating film is a silicon nitride film which grew through a plasma chemical vapor deposition process.

17. (Original) A method according to claim 16, wherein said silicon nitride film which grew through said plasma chemical vapor deposition process, is removed with an aqueous solution of hydrofluoric acid, using, as an etching stopper, said silicon nitride film which grew through said low-pressure chemical vapor deposition process.

18. (Original) A method according to claim 16, wherein the thickness of said silicon nitride film which grew through said plasma chemical vapor deposition process, is eight times or less that of said silicon nitride film which grew through said low-pressure chemical vapor deposition process.

19. (Original) A method according to claim 14, further comprising, after the step of selectively removing said third insulating film, the steps of:

forming a fourth insulating film so as to cover the exposed surfaces of said contact plug

and said spacer;

forming a second contact hole in said fourth insulating film so as to expose part of the surface of said contact plug and at least part of the side surface of said spacer;

forming a second conductive material on the side and bottom surfaces of said second contact hole;

selectively removing said fourth insulating film using an etchant whose etching rate to said second conductive material and said second insulating film is low.

20. (Original) A method according to claim 19, wherein said spacer is made of a conductive material and electrically connected to said second conductive material together with said contact plug.

21. (Original) A method according to claim 19, wherein said second conductive material is used as a storage node of DRAM.